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EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2628	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,485	BOOTH, LAWRENCE A.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-18 and 20-22* is/are rejected.

7)☒ Claim(s) *2,10 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 1, 3-9, 11-18, and 20-22 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments, see pages 4-8, filed March 7, 2007, with respect to the rejection(s) of claim(s) 1, 3-9, 11-18, and 20-22 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Pope (US005847705A).

3. With regard to Claims 1, 9, and 16, Applicant argues that Takala (US006909434B2) does not teach that that the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer. Takala states transferring the display information from the local frame buffer to the display frame buffer, but is silent with respect to maintenance of the same data in the local frame buffer and the display frame buffer (page 4).

In reply, the Examiner agrees that Takala does not appear to teach that the same display data is located in the local frame buffer and the display frame buffer at the same time. However, new grounds of rejection are made in view of Pope.

Applicant argues that it would not have been obvious to combine Yoshikawa (US006393520B2) and Takala because the arrangements of the components of

Yoshikawa are different than that of Takala. Consequently, it is submitted that the rejection entails hindsight (pages 5-6).

In reply, the Examiner disagrees. Takala is merely used for its teaching of only updating the display data in the internal frame buffer when a new frame is available in the external frame buffer (Col. 2, lines 1-19). It would have been obvious to incorporate this teaching into the device of Yoshikawa so that the display data in internal frame buffer is only updated when a new frame is available in the external frame buffer because this reduces the amount of transferring of the display data from the external memory to the internal memory since the display data is not transferred when the display contents are not changed, which reduces power consumption (Col. 1, lines 47-67; Col. 2, lines 1-19 in Takala).

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

4. With regard to Claims 5 and 21, Applicant argues that Yoshikawa and Takala fail to show the maintaining of display data in an external frame buffer as copied to an internal frame buffer (page 7).

In reply, the Examiner agrees that Takala does not appear to teach that the same display data is located in the internal frame buffer and the external frame buffer at the same time. However, new grounds of rejection are made in view of Pope.

Applicant argues that the video controller 10 of Yoshikawa does not appear to be a chip, but rather a circuit board that has several chips attached thereto. Applicant is unable to find any reference in Yoshikawa stating that the video controller may be a chip (page 7).

In reply, the Examiner disagrees. Yoshikawa discloses that the data processor (1, Figure 1) is a chip (Col. 5, lines 59-61). Figure 6 shows the video controller (10, Figure 6), to which the data processor of Yoshikawa's invention is applied (Col. 9, lines 5-8). Therefore, the video controller is one example of a data processor of Yoshikawa's invention, and since the data processor is a chip, this means that the video controller is a chip.

Applicant argues that Takala does not show an external frame buffer, as claimed. The local frame buffer 12 is incorporated in and thus, is not external to or separate from the ASIC. Applicant argues that no motivation has been provided to combine and modify Yoshikawa and Takala to arrive at the claimed invention (page 8).

In reply, the Examiner points out that Takala is merely used for its teaching of only updating the display data in the internal frame buffer when a new frame is available in the external frame buffer (Col. 2, lines 1-19). It would have been obvious to incorporate this teaching into the device of Yoshikawa so that the display data in internal frame buffer is only updated when a new frame is available in the external frame buffer because this reduces the amount of transferring of the display data from the external

memory to the internal memory since the display data is not transferred when the display contents are not changed, which reduces power consumption (Col. 1, lines 47-67; Col. 2, lines 1-19).

5. Applicant's arguments, see page 7, filed March 7, 2007, with respect to Claims 2, 10, and 19 have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejections of Claims 2, 10, and 19 has been withdrawn.

6. With regard to Claims 2, 10, and 19, Applicant argues that Yoshikawa discloses a data exchange the transfer of data from an external memory to an internal memory and vice versa, and does not teach display data that is copied into an internal frame buffer simultaneously with a display controller reading display data from an external frame buffer (page 7).

In reply, the Examiner agrees that Yoshikawa appears to teach that the display controller (13, 19, Figure 6) reads display data from the external frame buffer (14), then display data is transferred into the internal frame buffer (12) (*data stored in external memory 14 is being output through the D/A converter 19, data is then written into the internal memory 12*, Col. 9, lines 58-67), and does not appear to teach that this occurs simultaneously. Therefore, the rejections of these claims have been withdrawn.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "the internal frame buffer" and "the external frame buffer". There is insufficient antecedent basis for this limitation in the claim. Applicant is assumed to have meant "the internal *memory array*" and "the external *memory array*".

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 1, 3-8, 16-18, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa (US006393520B2) in view of Takala (US006909434B2), further in view of Pope (US005847705A).

12. With regard to Claim 1, Yoshikawa describes an apparatus comprising a processing unit (13, Figure 6) that decides which of frame buffers is being read or written (Col. 9, lines 16-18), and a D/A converter (19) outputs video data to a monitor from the frame buffers (Col. 9, lines 25-28). Therefore, the processing unit and D/A converter are considered to be a display controller. Yoshikawa describes an internal frame buffer (12) coupled to the display controller (*video controller 10 uses an internal memory 12 and an external memory 14 as frame buffers*, Col. 9, lines 6-8, *video data stored in the memories 12 and 14 are timely output through a D/A converter 19 so as to be displayed as video on a monitor,* Col. 9, lines 25-28); and a control circuitry (15) to copy display data from an external frame buffer (14) to the internal frame buffer, wherein the display data copied into the internal frame buffer is the same display data read by the display controller from the external frame buffer (Col. 9, lines 47-56; *transferring data from the external memory to the internal memory (first embodiment)*, Col. 7, lines 11-15; *in the same way as the first embodiment, data is exchanged between the internal and external memories 12 and 14*, Col. 9, lines 29-31, 58-67).

However, Yoshikawa does not teach that after the display data is copied, the same display data is located in the internal frame buffer until a new frame is available in the external frame buffer. However, Takala discloses that after the display data is copied from the external frame buffer (12, Figure 1) to the internal frame buffer (22), the internal frame buffer is only updated after a new frame is available in the external frame buffer (Col. 2, lines 1-19). Therefore, after the display data is copied, the same display data is located in the internal frame buffer until a new frame is available in the external frame buffer.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Yoshikawa so that after the display data is copied, the same display data is located in the internal frame buffer until a new frame is available in the external frame buffer as suggested by Takala. Takala suggests that two frame buffers are needed. One frame buffer is integrated in the display so that the display can be in a mobile electronic device (Col. 2, lines 1-3). The other frame buffer is an external frame buffer that is accessible by the software so that the software can change the contents of this frame buffer. The external frame buffer is copied to the integrated frame buffer to update the display (Col. 1, lines 12-22), and so the same display data is located in both frame buffers after the display is copied. The integrated frame buffer is only updated when a new frame is available in the external frame buffer because this reduces the amount of transferring of the display data from the external memory to the internal memory since the display data is not transferred when the display contents are not changed, which reduces power consumption (Col. 1, lines 47-67; Col. 2, lines 1-19).

However, Yoshikawa and Takala do not explicitly teach that the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer. Takala teaches that the display data is transferred from the external frame buffer to the internal frame buffer (Col. 1, lines 12-22), however Takala does not explicitly teach that the display data remains in the external frame buffer after it has been transferred. However, "transferring" data can mean that data is transferred from one frame buffer to another frame buffer so that there is a copy of the same data in each of the frame buffers. This is taught in Pope, as Pope discloses that the display data is transferred from the second frame buffer (18) to the first frame buffer (20), and a copy of the display data remains in the second frame buffer after it has been transferred (Col. 7, lines 36-49). Therefore, Pope discloses that the same display data is located in the first frame buffer (20) and the second frame buffer (18) until a new frame buffer is available in the second frame buffer (Col. 7, lines 36-49).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the internal (first) frame buffer and external (second) frame buffer of Takala so that the same display data is located in both frame buffers until a new frame is available in the second frame buffer as suggested by Pope because Pope suggests the same display data needs to be maintained in both frame buffers so that there is a reference means for detecting changes in the second frame buffer. Without the first frame buffer as a reference means for detecting changes in the second frame buffer, it would be necessary for the system to operate as if the entire contents of the second frame buffer were continuously changed. In that event, all memory locations of the external frame buffer would be continuously updated, even in those memory locations where no

display data change had occurred, resulting in substantial increase in overhead and degradation in system performance (Col. 8, lines 20-30). Therefore, Pope suggests the advantage of being able to compare the contents of the frame buffers so as to determine if the contents are different at any corresponding memory locations, and only copying the contents of the changed memory locations to the first frame buffer. Takala only teaches the ability to detect when the application updates the second frame buffer (Col. 2, lines 1-19), and therefore must transfer the entire contents of the second frame buffer to the first frame buffer since there is no way to detect which memory locations have changed since the same display data is not stored in both frame buffers at the same time. Therefore, it would be advantageous to modify the device of Takala with this teaching from Pope.

13. With regard to Claim 3, Yoshikawa does not teach that the display controller reads the display data from the internal frame buffer until the display controller receives a signal indicating that the external frame buffer contains the most recent display data. However, Takala describes reading the display data from the internal frame buffer (22, Figure 1) until receiving a signal indicating that the external frame buffer (12) contains the most recent display data (Col. 2, lines 1-19).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Yoshikawa so that the display controller reads the display data from the internal frame buffer until the display controller receives a signal indicating that the external frame buffer contains the most recent display data as suggested by Takala because Takala suggests that this reduces the amount of transferring of the display data from the external memory to the internal memory since the display

data is not transferred when the display contents are not changed, which reduces power consumption (Col. 1, lines 47-67).

14. With regard to Claim 4, Yoshikawa does not specifically teach that the display controller reads the display data from the internal frame buffer at least one time after a new frame display refresh operation. However, Takala describes reading the display data from the internal frame buffer (22, Figure 1) at least one time after a new frame display refresh operation (*updating said display frame buffer by transferring said display information from said local frame buffer to said display frame buffer, and display said display information on said display module*, Col. 2, lines 1-19).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Yoshikawa so that the display controller reads the display data from the internal frame buffer at least one time after a new frame display refresh operation as suggested by Takala because Takala suggests that it is advantageous for the display data to be read from the internal frame buffer for mobile devices and the display data is read from the internal frame buffer after a new frame display refresh operation so that the display data that is read is the updated display data (Col. 1, lines 6-24).

15. With regard to Claim 5, Yoshikawa discloses that the display controller (13, 19, Figure 6), the internal frame buffer (12) and the control circuitry (15) are disposed on a single graphics chip (10) and the external frame buffer (14) is disposed on another chip separate from the graphics chip, as shown in Figure 6. The data processor (1, Figure 1) is

a chip (Col. 5, lines 59-61). Figure 6 shows the video controller (10, Figure 6), to which the data processor of Yoshikawa's invention is applied (Col. 9, lines 5-8). Therefore, the video controller is one example of a data processor of Yoshikawa's invention, and since the data processor is a chip, this means that the video controller is a chip.

16. With regard to Claim 6, Yoshikawa describes that the display controller (13, 19, Figure 6), the internal frame buffer (12) and the control circuitry (15) are disposed on a single processor chip (10), as shown in Figure 6.

17. With regard to Claim 7, Yoshikawa describes that the control circuitry (15, Figure 6) comprises at least one register (16) to hold at least one data transaction of display data (*during the data exchange, a buffer register 16 of the memory control unit 15 is used as a data save storage, all data stored in the memory regions 17 and 18 are exchanged while partially saving data in the register 16*, Col. 9, lines 52-56).

18. With regard to Claim 8, Yoshikawa describes that the control circuitry (15, Figure 6) is to generate a write signal to be used by the internal frame buffer (12) based on an external memory (14) read signal and a memory clock signal (Col. 9, lines 47-52, 56-67).

19. With regard to Claim 16, Yoshikawa describes a method comprising reading display data from an external frame buffer (14, Figure 6) by a display controller (13, 19) during a new frame display refresh operation; and loading a copy of the display data from

the external frame buffer to an internal frame buffer (12) during the new frame display refresh operation (Col. 9, lines 57-67).

However, Yoshikawa does not teach that the same display data is located in the internal frame buffer until a new frame is available in the external frame buffer. However, Takala discloses that after the display data is copied from the external frame buffer (12, Figure 1) to the internal frame buffer (22), the internal frame buffer is only updated after a new frame is available in the external frame buffer (Col. 2, lines 1-19). Therefore, the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer. This would be obvious for the same reasons given in the rejection for Claim 1.

However, Yoshikawa and Takala do not teach that the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer. However, Pope discloses that the same display data is located in the first frame buffer (20) and the second frame buffer (18) until a new frame buffer is available in the second frame buffer (Col. 7, lines 36-49). This would be obvious for the same reasons given in the rejection for Claim 1.

20. With regard to Claim 17, Yoshikawa does not teach determining if a new frame is available in the external frame buffer; and reading the display data in the internal frame buffer by the display controller during subsequent display refresh operations if a new frame is not available in the external frame buffer. However, Takala describes determining if a new frame is available in the external frame buffer (12); and reading the display data in the internal frame buffer (22) during subsequent display refresh operations

if a new frame is not available in the external frame buffer (Col. 2, lines 1-19). This would be obvious for the same reasons given in the rejection for Claim 3.

21. With regard to Claim 18, Yoshikawa describes that the display data from the external frame buffer (14, Figure 6) includes rendered graphics objects or an entire frame (Col. 9, lines 6-8, 25-28).

22. With regard to Claim 20, Yoshikawa describes that loading of the data from the external frame buffer (14, Figure 6) to the internal frame buffer (12) is accomplished using data copy circuitry (15; Col. 9, lines 47-56).

23. With regard to Claim 21, Yoshikawa discloses disposing the display controller (13, 19, Figure 6), the internal frame buffer (12) and the data copy circuitry (15) on a single graphics chip (10); and disposing the external frame buffer (14) on another chip separate from the graphics chip, as shown in Figure 6. The data processor (1, Figure 1) is a chip (Col. 5, lines 59-61). Figure 6 shows the video controller (10, Figure 6), to which the data processor of Yoshikawa's invention is applied (Col. 9, lines 5-8). Therefore, the video controller is one example of a data processor of Yoshikawa's invention, and since the data processor is a chip, this means that the video controller is a chip.

24. With regard to Claim 22, Yoshikawa describes that loading of the data from the external frame buffer (14, Figure 6) to the internal frame buffer (12) further comprises temporarily storing at least one data transaction of the display data in a register (16; Col.

9, lines 52-56); and writing the stored data into the internal frame buffer based on an external memory read signal (Col. 9, lines 57-67).

25. Claims 9, 11 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa (US006393520B2) in view of Takala (US006909434B2), further in view of Cross (US006108015A), further in view of Pope (US005847705A).

26. With regard to Claim 9, Yoshikawa describes a system comprising a display device; a graphics chip (10, Figure 6) coupled to the display device, the graphics chip including display controller (13, 19), an internal memory array (12) (Col. 9, lines 6-8, 16-18, 25-28) and data copy circuitry (15; Col. 9, lines 47-56); and an external memory array (14; Col. 9, lines 6-8) disposed on another chip separate from the graphics chip, as shown in Figure 6, wherein the data copy circuitry is coupled between the external memory array and the internal memory array to enable data from the external memory array to be copied to the internal memory array (Col. 9, lines 47-56; Col. 7, lines 11-15; Col. 9, lines 29-31, 58-67).

However, Yoshikawa does not teach that the data from the external memory array is copied to the internal memory array during a new frame display refresh operation, wherein after the display data is copied, the same display data is located in the internal frame buffer until a new frame is available in the external frame buffer, and wherein subsequent display refresh operations are accomplished by the display controller retrieving data from the internal memory array until a new frame is available in the external memory array. However, Takala describes that the data from the external

memory array (12) is copied to the internal memory array (22) during a new frame display refresh operation, wherein subsequent display refresh operations are accomplished by retrieving data from the internal memory array until a new frame is available in the external memory array (Col. 2, lines 1-19). After the display data is copied from the external frame buffer (12, Figure 1) to the internal frame buffer (22), the internal frame buffer is only updated after a new frame is available in the external frame buffer (Col. 2, lines 1-19). Therefore, after the display data is copied, the same display data is located in the internal frame buffer until a new frame is available in the external frame buffer. This would be obvious for the same reasons given in the rejections for Claims 1 and 3.

However, Yoshikawa and Takala do not specifically teach that the graphics chip is coupled between the processor and the display device. However, Cross describes that the graphics chip (107, Figure 1) is coupled between the processor (101) and the display device (106) (Col. 4, lines 37-46).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Yoshikawa and Takala so that the graphics chip is coupled between the processor and the display device as suggested by Cross because Cross suggests that a processor is needed to control the overall operation of the system (Col. 4, lines 47-50).

However, Yoshikawa, Takala, and Cross do not teach that the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer. However, Pope discloses that the same display data is located in the first frame buffer (20) and the second frame buffer (18) until a new

frame buffer is available in the second frame buffer (Col. 7, lines 36-49). This would be obvious for the same reasons given in the rejection for Claim 1.

27. With regard to Claim 11, Yoshikawa describes that the display data copied into the internal memory array (12, Figure 6) is the same display data read by the display controller (13, 19) from the external memory array (14) (Col. 9, lines 57-67).

28. With regard to Claim 13, Yoshikawa describes that the data copy circuitry (15, Figure 6) comprises at least one register (16) to hold at least one data transaction of display data (Col. 9, lines 51-56).

29. With regard to Claim 14, Yoshikawa describes that the data copy circuitry (15, Figure 6) generates a write signal to be used by the internal memory array (12) based on an external memory (14) read signal and a memory clock signal (Col. 9, lines 47-52, 56-67).

30. With regard to Claim 15, Yoshikawa does not teach a portable power source coupled to power the display controller, the internal memory array, the external memory array and the data copy circuitry. However, Takala describes a portable power source coupled to power (Col. 1, lines 59-62) the display (24, Figure 1), the internal memory array (22), and the external memory array (12) (Col. 2, lines 1-19).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Yoshikawa to include a portable power

source as suggested by Takala because Takala suggests the advantage of being able to use this display in a mobile device (Col. 1, lines 59-62).

31. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa (US006393520B2), Takala (US006909434B2), Cross (US006108015A), and Pope (US005847705A) in view of Aleksic (US 20040150647A1).

Yoshikawa, Takala, Cross, and Pope are relied upon for the teachings as discussed above relative to Claim 9.

However, Yoshikawa, Takala, Cross, and Pope do not specifically teach that a graphics generator is disposed on the graphics chip. However, Aleksic describes that a graphics generator (310, Figure 3) is disposed on the graphics chip (118; graphics system 118 includes a graphics engine 310, [0021-0022] components of the graphics system 118 are formed on a common semiconductor, [0018], lines 18-21).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yoshikawa, Takala, Cross, and Pope so that as a graphics generator is disposed on the graphics chip suggested by Aleksic because Aleksic suggests that a graphics generator is needed to process graphics commands such as bitblt, scaling, object rotation, alpha blending, and anti-aliasing commands [0022], and it would be advantageous to have to the graphics generator on the graphics chip to save power, because accessing components outside of the graphics chip requires additional power ([0018], lines 25-30).

Allowable Subject Matter

32. Claims 2, 10, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

33. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken singly or in combination do not teach or suggest an apparatus comprising a display controller; an internal frame buffer coupled to the display controller; a control circuitry to copy display data from an external frame buffer to the internal frame buffer, wherein the display data copied into the internal frame buffer is the same display data read by the display controller from the external frame buffer, wherein after the display data is copied, the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer; and wherein the display data is copied into the internal frame buffer **simultaneously** with the display controller reading the display data from the external frame buffer, as recited in each of Claims 2, 10, and 19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

KEE M. TUNG
SUPERVISORY PATENT EXAMINER